IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Claim 1. (Original) A method for forming a semiconductor device comprising the steps:

providing a substrate including a support region and an array region having an array device diffusion region;

depositing a dielectric layer on said substrate;

forming a patterned hardmask on said dielectric layer, said patterned hardmask having a first opening that overlays at least a portion of said array device diffusion region;

partially etching said dielectric layer selective to said hardmask through said first opening to form a first recess in said dielectric layer;

forming a second mask having a second opening at least partially overlapping a portion of said first recess; and

subsequently etching said dielectric layer selective to said hardmask through said second opening and through said portion of said first recess,

so that said portion of said first recess is extended through said dielectric layer to form a second recess so that a corresponding portion of said array device diffusion region is exposed.

Claim 2. (Original) The method of claim 1, further comprising, after said step of subsequently etching:

removing said second mask;

forming a first conductive feature in said second recess; and

forming a second conductive feature in said first recess.

Claim 3. (Original) The method of claim 1 wherein said second mask further comprises a block mask over said support region.

Claim 4. (Original) The method of claim 2 wherein said first conductive feature comprises a contact structure and said second conductive feature comprises an interconnect structure.

Claim 5. (Original) The method of claim 1 wherein said second opening defines a contact via.

Claim 6. (Original) The method of claim 1 wherein said patterned hardmask defines an interconnect feature, and said second mask comprises a line-type opening that is oriented to intersect said interconnect feature at an angle.

Claim 7. (Original) The method of claim 6 wherein said angle is approximately 90 degrees.

Claim 8. (Original) The method of claim 1 wherein said second mask is completely open in said array region.

Claim 9. (Original) The method of claim 3 wherein said second mask is completely open in said array region.

Claim 10. (Original) The method of claim 1 wherein said array region further comprises a memory device corresponding to said array device diffusion region.

Claim 11. (Original) The method of claim 10 wherein said memory device comprises a gate stack including an encapsulating dielectric positioned adjacent to said array device diffusion region, and wherein said method further comprises filling said second recess with a conductive material to form a borderless contact.

Claim 12. (Original) The method of claim 10 wherein said memory device further comprises a vertical transistor.

Claim 13. (Original) The method of claim 1 wherein said support region includes

a support device diffusion region, wherein said patterned hardmask includes a third opening that overlays at least a portion of said support device diffusion region and

said step of partially etching further comprises simultaneously etching through said third opening to form a third recess, and

wherein said second mask further comprises a fourth opening at least partially overlapping a portion of said third recess and

said step of subsequently etching further comprises simultaneously etching through said fourth opening and through said portion of said third recess

so that said portion of said third recess is extended through said dielectric layer to form a fourth recess so that a

corresponding portion of said support device diffusion region is exposed.

Claim 14. (Original) The method of claim 13, further comprising, after said step of subsequently etching:

removing said second mask;

depositing a conductive material in said second recess and said fourth recess to form contact structures; and

depositing a second conductive material in said first recess and said third recess to form interconnect structures.

Claims 15-20. (Canceled)